AMENDMENTS TO THE CLAIMS

The following listing of claims replaces all prior listings of claims in the present application.

What is claimed is:

1. (Currently Amended) A semiconductor integrated circuit, comprising:

a silicon substrate;

a silicon epitaxial layer that ~~touches the surface of said silicon substrate and~~ has a lower resistivity than the resistivity of said silicon substrate;

first and second circuit sections formed in said silicon epitaxial layer; and

a device isolation region projecting from said silicon substrate up to a surface of each of said first and second circuit sections between said first and second circuit sections wherein the portions of the epitaxial layer under both the first and second circuits are in contact with the substrate .

2. (Previously Presented) The semiconductor integrated circuit according to Claim 1, wherein the resistivity of said silicon substrate is between 20 and 100 times the resistivity of said silicon epitaxial layer.

3. (Previously Presented) The semiconductor integrated circuit according to Claim 2, wherein the resistivity of said silicon substrate is between 50 and 100 times the resistivity of said silicon epitaxial layer.

4. (Canceled).

5. (Previously Presented) The semiconductor integrated circuit according to Claim 1, wherein a digital circuit is formed on said firs circuit section, and an analog circuit is formed on said second circuit section.

6-10. (Cancelled)

11. (Previously Presented) The semiconductor integrated circuit according to Claim 1, wherein said silicon epitaxial layer is a single layer.

12. (Previously Presented) The semiconductor integrated circuit according to Claim 1, wherein said silicon epitaxial layer is a p-type bulk epitaxial layer.

13. (Previously Presented) The semiconductor integrated circuit according to Claim 12, wherein said silicon substrate comprises a p-type bulk substrate.

14. (Previously Presented) The semiconductor integrated circuit according to Claim 13, wherein a first impurity concentration of the p-type bulk substrate is one-hundredth or less a second impurity concentration of the p-type bulk epitaxial layer.

15. (Previously Presented) The semiconductor integrated circuit according to Claim 13, wherein said silicon substrate has a thickness of 0.7mm and a resistivity of 1000 Ohm – cm.

16. (Previously Presented) The semiconductor integrated circuit according to Claim 12, wherein said p-type bulk epitaxial layer is formed by a chemical vapor deposition method.

17. (Previously Presented) The semiconductor integrated circuit according to Claim 12, wherein said silicon epitaxial layer has a thickness of 5 micrometers and a resistivity of 10 Ohm – cm.

18. (New) The semiconductor integrated circuit according to Claim 1, wherein said silicon substrate and said silicon epitaxial layer are of the same conductivity type.